PAT-003-1152004 Seat No. _____

M. Sc. (Electronics) (Sem. II) (CBCS) Examination

August / September - 2020

Advance Digital Electronics : Paper - 8

(New Syllabus)

Faculty Code : 003

Subject Code : 1152004

Time : $2\frac{1}{2}$ Hours] [Total Marks : **70**

1 Answer the following : (Any 7 out of 10) **14**

(1) Name the PLD which has

(a) Programmable AND array at the input and a Fixed OR array at the output.

(b) Fixed AND array at the input and a Programmable OR array at the output.

(2) Differentiate between Synchronous and Asynchronous Counters. (2 points each).

(3) What is a Flip-Flop ? Explain.

(4) Determine the size of PROM required for implementing the following logic circuits.

(a) A single digit BCD adder/subtractor with a control input for selection of operation.

(b) 16 to 1 multiplexer

(5) Fill in the blanks :

(a) _____ has the highest priority in 8085 interrupts.

(b) Microprocessor 8085 has _____ and _____ pin (name) for serial communication.

(6) Enlist all registers available in 8085.

(7) With the help of block diagram, Show J - K Flip Flop as D type and T type Flip Flop. Write their truth table.

(8) List the types of Shift Registers.

(9) Explain working of R - S Flip Flop as switch de bouncer.

(10) Implement Boolean expression $f(A,B,C) = \Sigma(1,2,4,7)$ using $M \cup X$ 4 to 1.

2 Answer the following : (Any 2 out of 3) 14

(1) Implement the following Boolean expression using PROM.

F1 (A,B,C,D) = Σ (0,2,5,9,12,13)

F2 (A,B,C,D) = Σ (1,3,6,8,10,11)

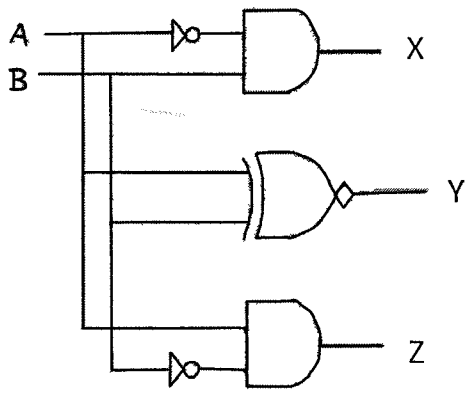
F3 (A,B,C,D) = Σ (6,7,8,12,14,15)

(2) Design a four line to two line priority encoder with active High inputs and outputs, with priority assigned to the higher order data input line.

(3) Draw the internal architecture of microprocessor 8085. Explain its General purpose registers.

3 Answer the following : 14

(1) Identify and explain the output of following circuit.



(2) Design and explain 4 to 16 decoder with two 3 to 8 decoders having an active LOW ENABLE inputs.

OR

3 Answer the following : 14

(1) Design and explain 4 bit Ring Counter with block diagram and timing waveforms.

(2) Design and explain Negative edge triggered J - K flip - flop with ACTIVE HIGH inputs.

4 Answer the following : **14**

(1) Explain each of the following codes and final result of all used registers.

Memory	data
8000	36H
8001	55H
8002	FFH

CODES :

```
LXI H 8000H
MOV A, M
INX H
MOV B, M
ADD B
INR B
RLC
INX H
MOV M, A
HLT
```

(2) Design and explain 4 bit ASYNCHRONOUS Binary Counter with logic diagram and necessary waveforms.

5 Answer the following : (Any 2 out of 4) **14**

(1) With the help of logic diagram and the truth table, describe the operation of a clocked R - S flip - flop with active HIGH R & S inputs. (clock is positive level trigger)

(2) Design mod 12 UP counter using IC 74293 and DOWN counter using IC 74193.

(3) Write a note on Programmable Logic Devices.

(4) Design and explain 1 Digit BCD adder circuit using IC 7483.
